



Description

JMT N-channel Enhancement Mode Power MOSFET

Features

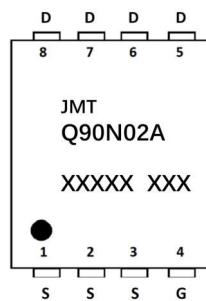
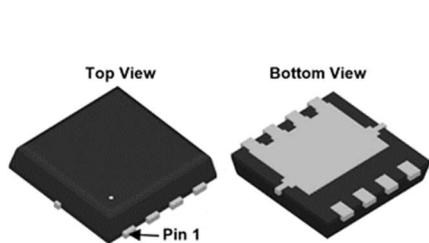
- 20V, 60A
- $R_{DS(ON)} < 4.0\text{m}\Omega$ @ $V_{GS} = 4.5\text{V}$
- $R_{DS(ON)} < 6.0\text{m}\Omega$ @ $V_{GS} = 2.5\text{V}$
- Lead free and Green Device Available
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

- Load Switch
- PWM Application
- Power management

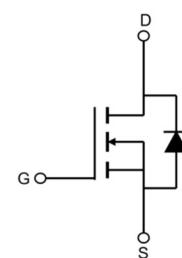


100% UIS TESTED!
100% ΔV_{ds} TESTED!



PDFN3.3X3.3-8L

Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
JMTQ90N02A	JMTQ90N02A	TAPING	PDFN3.3X3.3-8L	13inch	5000	50000

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Max.		Units
V_{DSS}	Drain-Source Voltage		20		V
V_{GSS}	Gate-Source Voltage		± 12		V
I_D	Continuous Drain Current		$T_A = 25^\circ\text{C}$		60
			$T_A = 100^\circ\text{C}$		39
I_{DM}	Pulsed Drain Current ^{note1}		240		A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		110		mJ
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	26		W
$R_{\theta JC}$	Thermal Resistance, Junction to Ambient		4.3		$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		$^\circ\text{C}$

**Electrical Characteristics** ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS}=\pm 12\text{V}$, $V_{DS}=0\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	0.4	0.7	1.0	V
$R_{DS(\text{on})}$ note3	Static Drain-Source On-Resistance	$V_{GS}=4.5\text{V}$, $I_D=30\text{A}$	-	2.8	4	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}$, $I_D=20\text{A}$		4	6	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=10\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	3200	-	pF
C_{oss}	Output Capacitance		-	460	-	pF
C_{rss}	Reverse Transfer Capacitance		-	445	-	pF
Q_g	Total Gate Charge	$V_{DS}=10\text{V}$, $I_D=30\text{A}$, $V_{GS}=4.5\text{V}$	-	48	-	nC
Q_{gs}	Gate-Source Charge		-	3.6	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	19	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=10\text{V}$, $I_D=30\text{A}$, $R_G=1.8\Omega$, $V_{GS}=4.5\text{V}$	-	9.7	-	ns
t_r	Turn-On Rise Time		-	37	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	63	-	ns
t_f	Turn-Off Fall Time		-	52	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current		-	-	90	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	360	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$, $I_{SD}=30\text{A}$, $T_J=25^\circ\text{C}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$T_J=25^\circ\text{C}$, $I_F=30\text{A}$, $dI/dt = 100\text{A}/\mu\text{s}$	-	23	-	ns
Q_{rr}	Reverse Recovery Charge		-	10	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J=25^\circ\text{C}$, $V_{DD}=15\text{V}$, $V_G=4.5\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{AS}=21\text{A}$ 3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

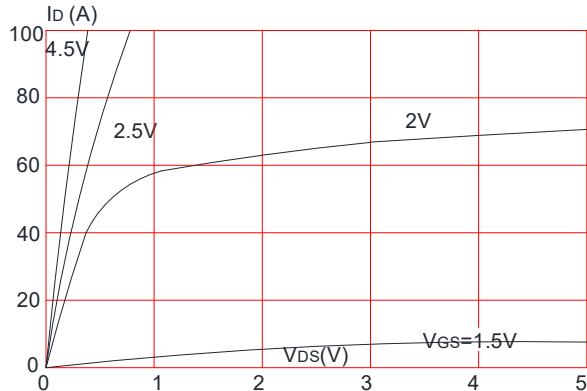


Figure 3: On-resistance vs. Drain Current

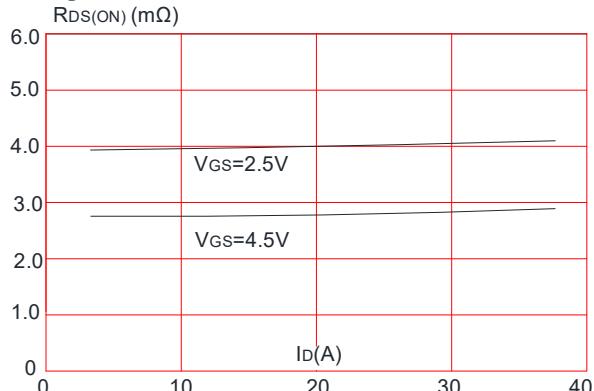


Figure 5: Gate Charge Characteristics

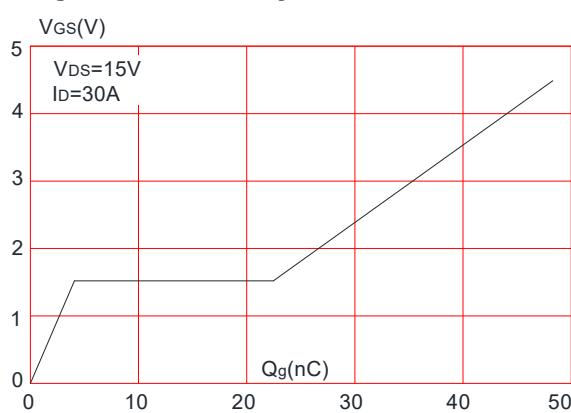


Figure 2: Typical Transfer Characteristics

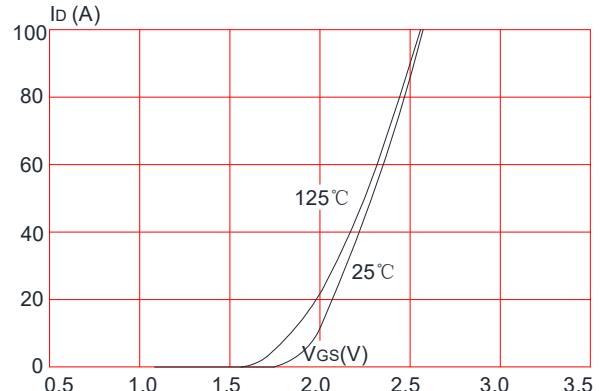


Figure 4: Body Diode Characteristics

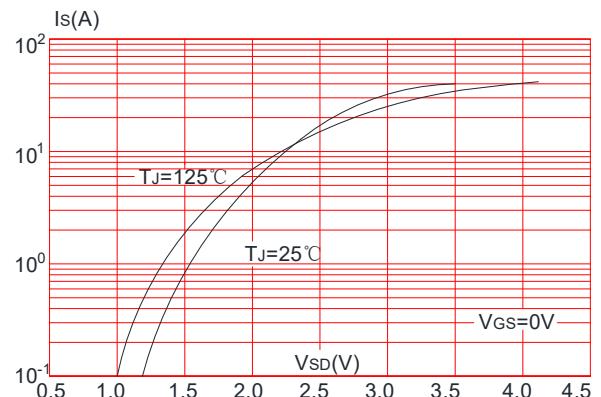


Figure 6: Capacitance Characteristics

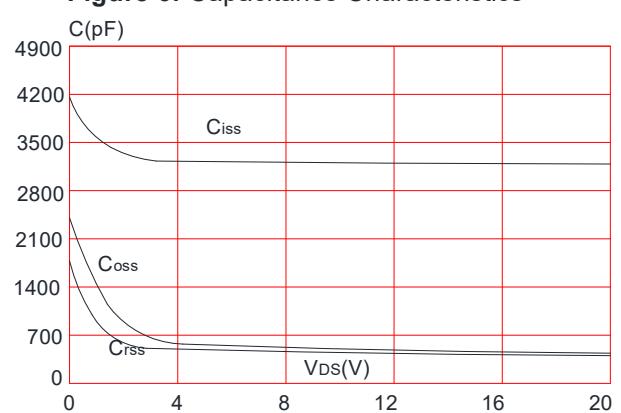


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

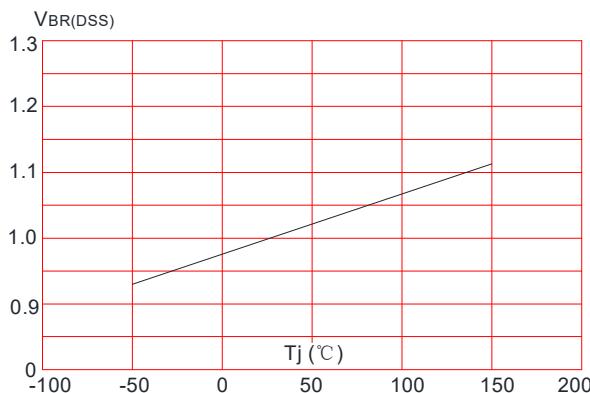


Figure 8: Normalized on Resistance vs. Junction Temperature

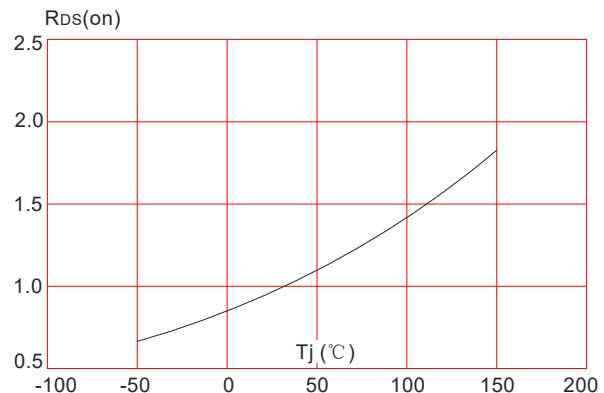


Figure 9: Maximum Safe Operating Area

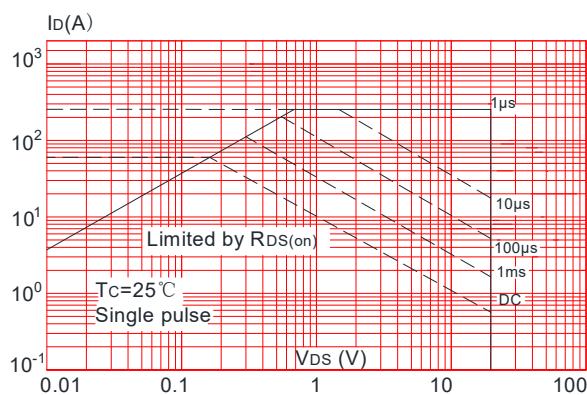


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

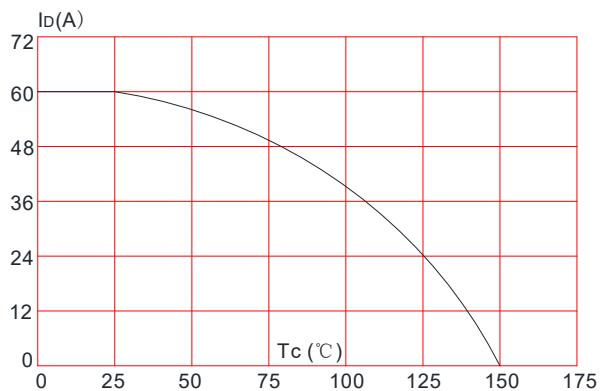
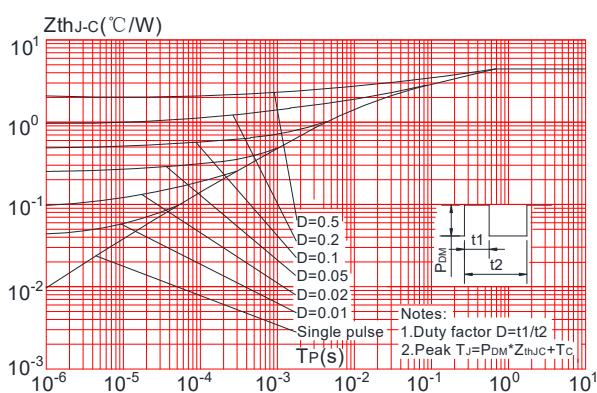


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuit

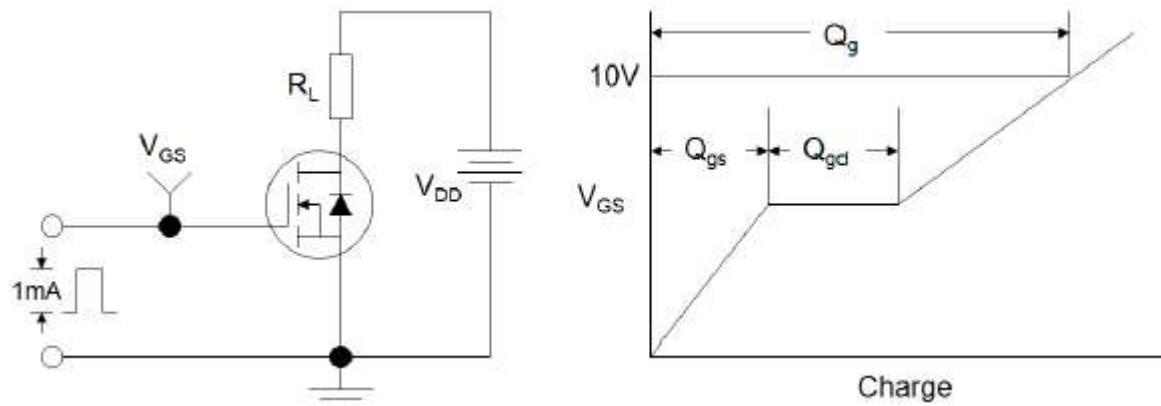


Figure1:Gate Charge Test Circuit & Waveform

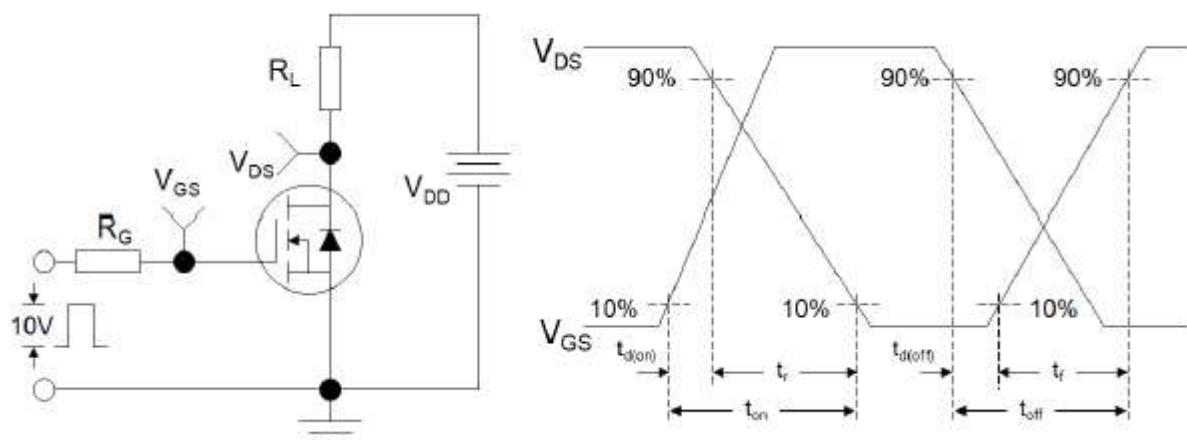


Figure 2: Resistive Switching Test Circuit & Waveforms

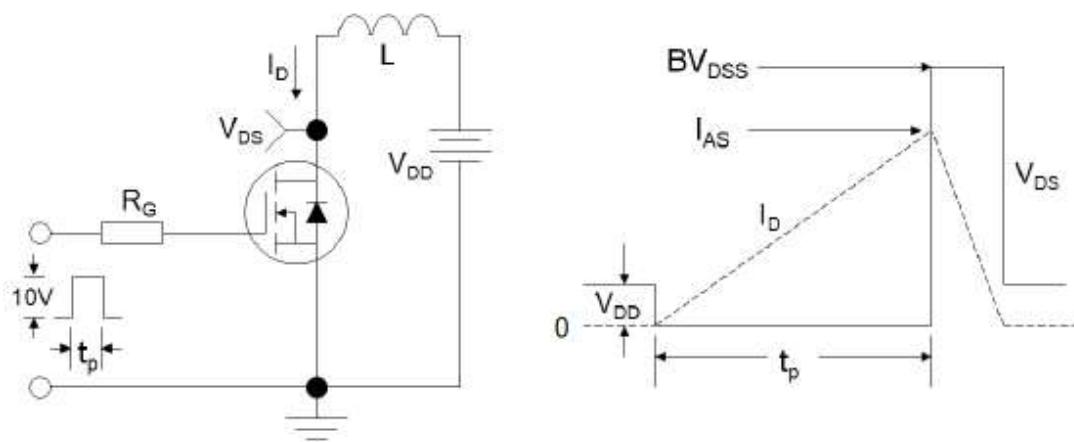
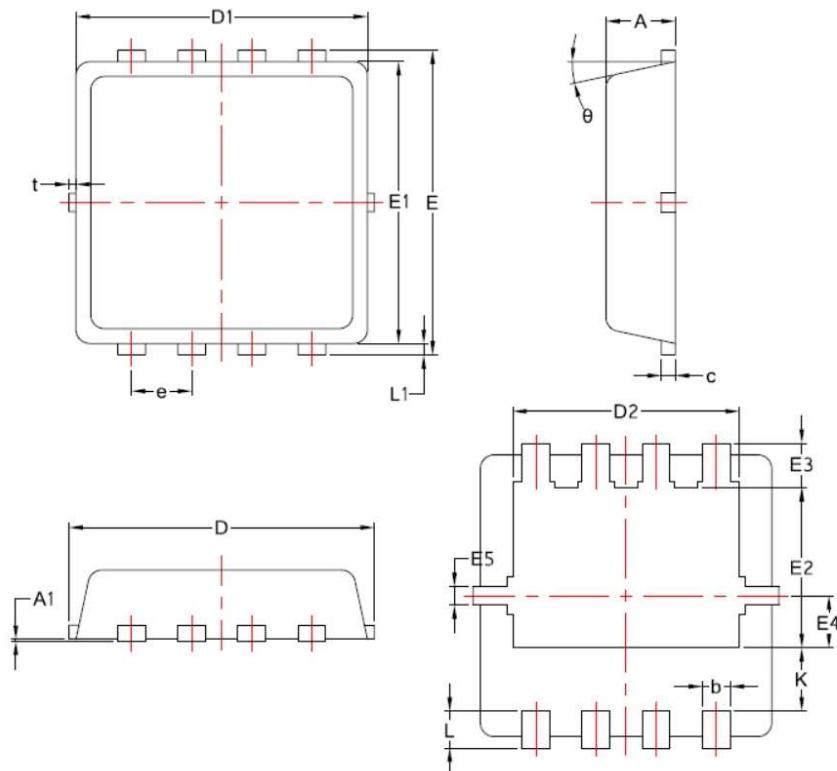


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

Package Mechanical Data- PDFN3.3X3.3-8L



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
θ	10°	12°	14°

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